

9 second output driver circuitry to output data onto a first  
10 external signal line wherein:

11 the second output driver circuitry outputs a first  
12 portion of data in response to a rising edge transition of a  
13 first external clock signal and the second output driver  
14 circuitry outputs a second portion of data in response to a  
15 falling edge transition of the first external clock signal.

1 <sup>22</sup>  
<sup>172</sup>. (Amended) The integrated circuit device of claim <sup>18</sup> ~~168~~  
2 wherein [the] a clock alignment circuit generates an internal clock  
3 signal, and the first output driver circuitry and the second output  
4 driver circuitry output [outputs] data in response to the internal  
5 clock signal.

In claim 174, lines 3, 7, and 11, before "output" insert  
--first--.

In claim 175, line 5, before "output" insert --first--.

In claim 176, line 4, before "output" insert --first--.

1 <sup>27</sup>  
<sup>177</sup>. (Amended) The integrated circuit device of claim <sup>24</sup> ~~174~~  
2 [176] further including a clock alignment circuit [coupled to the  
3 first external clock signal, the clock alignment circuit] to  
4 generate a first internal clock signal using the first external  
5 clock signal, wherein the multiplexer circuitry couples the first  
6 portion of data to the input of the first output driver circuitry  
7 in response to the first internal clock signal.